

WEST Search History

DATE: Friday, June 09, 2006

Hide?	<u>Set Name</u>	<u>Query</u>	<u>Hit Count</u>
		<i>DB=PGPB,USPT; PLUR=NO; OP=ADJ</i>	
<input type="checkbox"/>	L38	compiler with l31	1
<input type="checkbox"/>	L37	identif\$3 with l31	1
<input type="checkbox"/>	L36	recogniz\$3 with l31	1
<input type="checkbox"/>	L35	test\$3 with l31	2
<input type="checkbox"/>	L34	illegal instruction\$1 with test\$3	25
<input type="checkbox"/>	L33	unsupported with instruction\$1 with test\$3	0
<input type="checkbox"/>	L32	test\$3 with L31	2
<input type="checkbox"/>	L31	unsupported feature\$1	83
<input type="checkbox"/>	L30	unsupported feature\$1\$1	83
<input type="checkbox"/>	L29	unsupported instruction\$1	10
<input type="checkbox"/>	L28	illegal instruction\$1	577
<input type="checkbox"/>	L27	instruction with L26	18
<input type="checkbox"/>	L26	test\$3 with processor with capabilit\$3	368
<input type="checkbox"/>	L25	compiler with l12	1
<input type="checkbox"/>	L24	L12 with instruction\$1	35
<input type="checkbox"/>	L23	intel.asn. and L12	16
<input type="checkbox"/>	L22	L14 and L12	0
<input type="checkbox"/>	L21	(audio same chipset) and L17	11
<input type="checkbox"/>	L20	(audio and chipset) and L18	4
<input type="checkbox"/>	L19	(audio same chipset) and L18	0
<input type="checkbox"/>	L18	intel.asn. and L17	8
<input type="checkbox"/>	L17	input-output with chipset	107
<input type="checkbox"/>	L16	join and L14	7
<input type="checkbox"/>	L15	join same L14	2
<input type="checkbox"/>	L14	fork with L13	27
<input type="checkbox"/>	L13	thread\$1 with speculat\$3	294
<input type="checkbox"/>	L12	detect\$3 with processor with capabilit\$3	699
<input type="checkbox"/>	L11	(mch) and intel.as	0
<input type="checkbox"/>	L10	(memory controller hub) and intel.as	0
<input type="checkbox"/>	L9	intelligent hub and intel.as	0
<input type="checkbox"/>	L8	intelligent hub and intel.as	0

└	L7	intel.as. and L6	36
└	L6	system bus same memory controller same bus bridge	1604
└	L5	intel.as. and L4	57
└	L4	processors with L3	238
└	L3	front side bus	1072
└	L2	processors with L1	5
└	L1	north with south with bridge with bus	573

END OF SEARCH HISTORY